



John Burke Vietnam LLC

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PCBDFM

User Manual

ODB++ copper balance and design-for-manufacture review

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Web app: <https://pcbdfm.pplx.app>

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1. Introduction

PCBDFM checks a printed circuit board design for manufacturability before it is released to a fabricator. You give it the ODB++ job exported from your CAD system, and it reads the real copper, drill and solder-mask geometry of every layer — pads, lines, arcs, surfaces and negative features — clipped to the board outline and tagged by net.

It works in two stages:

- **Copper balance (automatic).** As soon as the job is read, PCBDFM measures the copper coverage and copper weight of every layer from L1 to the last layer, the copper area and mass, and how well each mirrored pair of layers balances. Unbalanced copper is a main cause of bow and twist after lamination and reflow.
- **DFM full design review (on request).** One click runs the complete manufacturability review: drill basis, via spans and aspect ratios, annular rings and drill breakout, hole-wall clearances, copper-to-copper spacing per layer against the copper weight, board edge, stack-up and prepreg resin fill, solder mask and data completeness. Each finding is graded and comes with a recommended fix.

The review can be run against typical fab capability, against a specific vendor's capability file, or against values you type in. Results can be downloaded as PDF reports and Excel workbooks for the design team and the fabricator.

Beta release. This is PCBDFM BETA version 1.0.57. The version is shown next to the name at the top of the page and in the footer of every report. Rules marked "typical" are screening values, not IPC-specified limits — confirm findings with your fabricator before changing a released design.

2. Getting started

Web address

Open <https://pcbdfm.pplx.app> in a current version of Chrome, Edge, Firefox or Safari. No account or installation is needed.

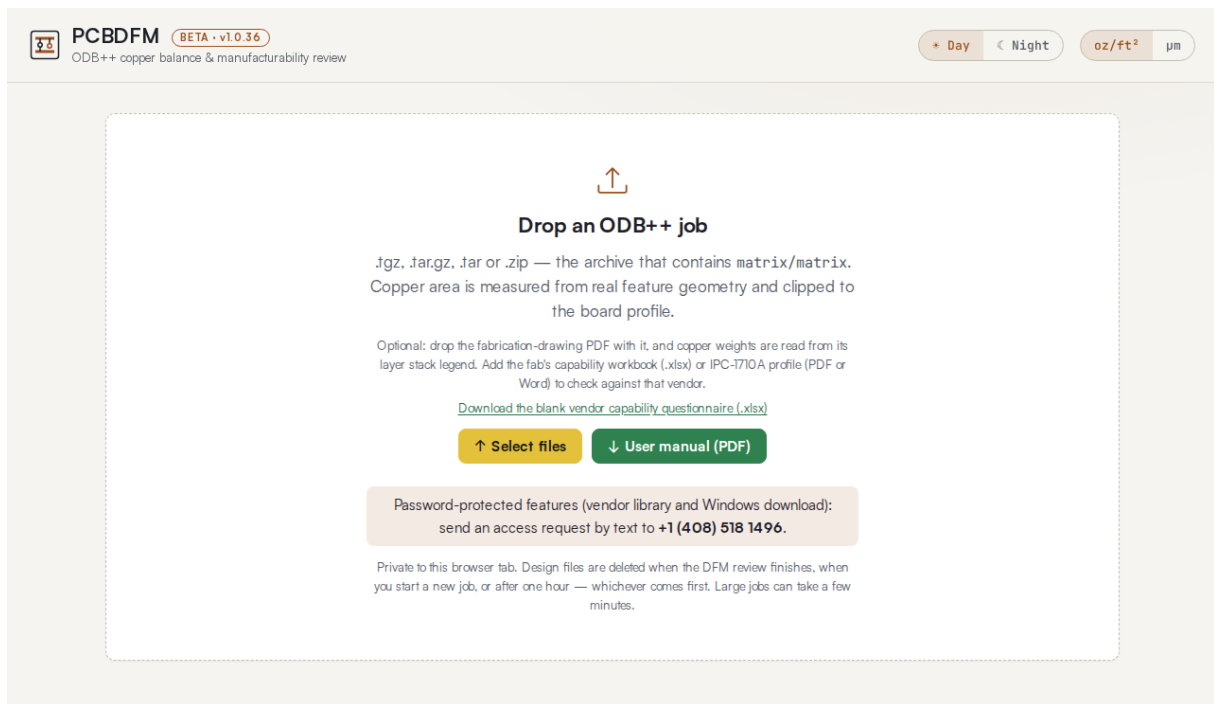


Figure 1 — The PCBDFM start page

- **User manual:** the green User manual (PDF) button on the start page downloads this manual, on the website and in the Windows app.
- **Access requests:** the vendor library and the Windows download are password protected. To request access, send a text to +1 (408) 518 1496. The note on the start page gives the same number.

Privacy

- Each browser tab is a private session. Other users never see your job, your results or your files.
- Design files are deleted when the DFM review finishes, when you start a new job, or after one hour — whichever comes first.
- Refreshing the page or opening the address in a new tab always starts a fresh, empty session.
- The website keeps anonymous usage counts for John Burke Vietnam LLC — how many times the page is opened, jobs analysed, reviews run and reports downloaded. Only numbers are kept: no file names, job names, design data or IP addresses. The Windows desktop app counts nothing.

Desktop app for Windows

PCBDFM is also available as a Windows desktop app (Windows 10 or 11, 64-bit). It uses the same engine and page, but runs entirely on your own PC — nothing is uploaded. Download it from the bottom of the web page; a download password is required, available from John Burke Vietnam LLC.

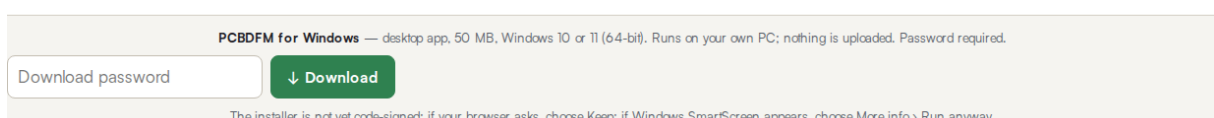


Figure 2 — Desktop app download

The installer is not yet code-signed. If your browser asks, choose Keep; if Windows SmartScreen appears, choose More info › Run anyway. After installation, start PCBDFM from the Start menu; your browser opens the app at a local address on your PC.

3. Files you can upload

Click Select files, or drag files onto the drop area. You can drop several files together — for example the ODB++ job, the fabrication drawing and the vendor's capability file in one go.

File	Formats	What PCBDFM uses it for
ODB++ job (required)	.tgz, .tar.gz, .tar, .zip — up to 512 MB	The archive exported from the CAD system that contains matrix/matrix. All layers, drills, nets, profile, stack-up attributes and drill tables are read from it. Compressed feature files inside the archive (.z, .Z, .gz) are expanded automatically.
Fabrication drawing (optional)	.pdf	Two things are read from the drawing: copper weights from the layer stack legend, and the drill table. When the drill table (or a drawing note) says the hole sizes are finished, plated holes are assessed with an oversized drill to allow for plating. Can also be added later with the Stackup PDF... button.
Vendor capability workbook (optional)	.xlsx, .xlsm	The fabricator's completed PCB Fabrication Capability Questionnaire. Its limits and its trace/space, drill and aspect-ratio tables are used for the DFM review.
Vendor IPC-1710A profile (optional)	.pdf, .docx, .doc	The fabricator's IPC-1710A capability profile. Its limits are extracted and used for the DFM review.

Drawing check. When a fabrication drawing is added, a message below the job summary confirms what was read from it: how many layers took their copper weight from the stack legend, and whether a drill table with finished hole sizes was found. Add the drawing before running the DFM review.

No layer stack legend matching this job's layer names was found in the PDF. Drill table: 5 hole sizes listed as FINISHED (mm drawing) — the DFM review drills plated holes 0.05 mm larger to allow for plating; non-plated holes as listed (a drill table inside the ODB++ job takes priority).

Figure 3 — Message after a fabrication drawing is read

Blank questionnaire. The link Download the blank vendor capability questionnaire (.xlsx) on the start page gives you an empty workbook to send to a fabricator. When it comes back completed, drop it in with the job.

Not accepted. Gerber, Excellon-only drill files, IPC-2581 and native CAD files cannot be read; export ODB++ from your CAD tool first (Cadence Allegro, Mentor/Siemens, Altium and KiCad all export ODB++).

4. Stage 1 — Copper balance (automatic)

After upload, progress is shown while the archive is unpacked and the copper features are merged layer by layer: the panel names the layer being worked on (for example “Copper layer 5 of 14 — L05_PWR1”) and the time elapsed. The copper balance then appears automatically — there is nothing else to click.

- **Large jobs:** analysis time grows with the amount of copper detail. A 2.5 MB, 14-layer job takes about 20 seconds; a 50 MB job can take 10 minutes or more. Keep the tab open while it runs. If the website reports that a job is too large for the server memory, use the PCBDFM Windows app, which uses your own PC.
- **Negative plane layers:** some CAD tools (Allegro in particular) write ground and power planes as negative layers, where the file draws the clearances and plane splits instead of the copper. PCBDFM reads the layer polarity from the job and, for a negative layer, reports copper as the board area minus the clearances drawn. A note under the copper balance lists these layers.
- **Negative planes in the DFM review:** the review checks negative plane layers too. The copper checked is the board area minus the clearances drawn, so anti-pad clearance to other-net holes, rings on connected holes and plane-split gaps are all measured. Each plane area takes the net of the plated holes connected to it; a plane area no plated hole connects to is reported as copper with no net.
- **Large boards:** the review reads, checks and releases one copper layer at a time, so memory is set by the largest layer, not the whole job. Negative planes and layers with more than 100,000 features are checked in overlapping tiles; every check distance is shorter than the overlap, so the results are the same. A large board takes longer: a 22-layer board with about 3 million copper features and 96,000 holes takes 35 to 60 minutes, depending on the computer, and the progress line shows the layer being checked and the time so far. The server reviews one large board at a time; a second waits and says so. A single layer above 1.5 million features is not reviewed, and the DFM panel gives the reason as soon as the copper balance appears.

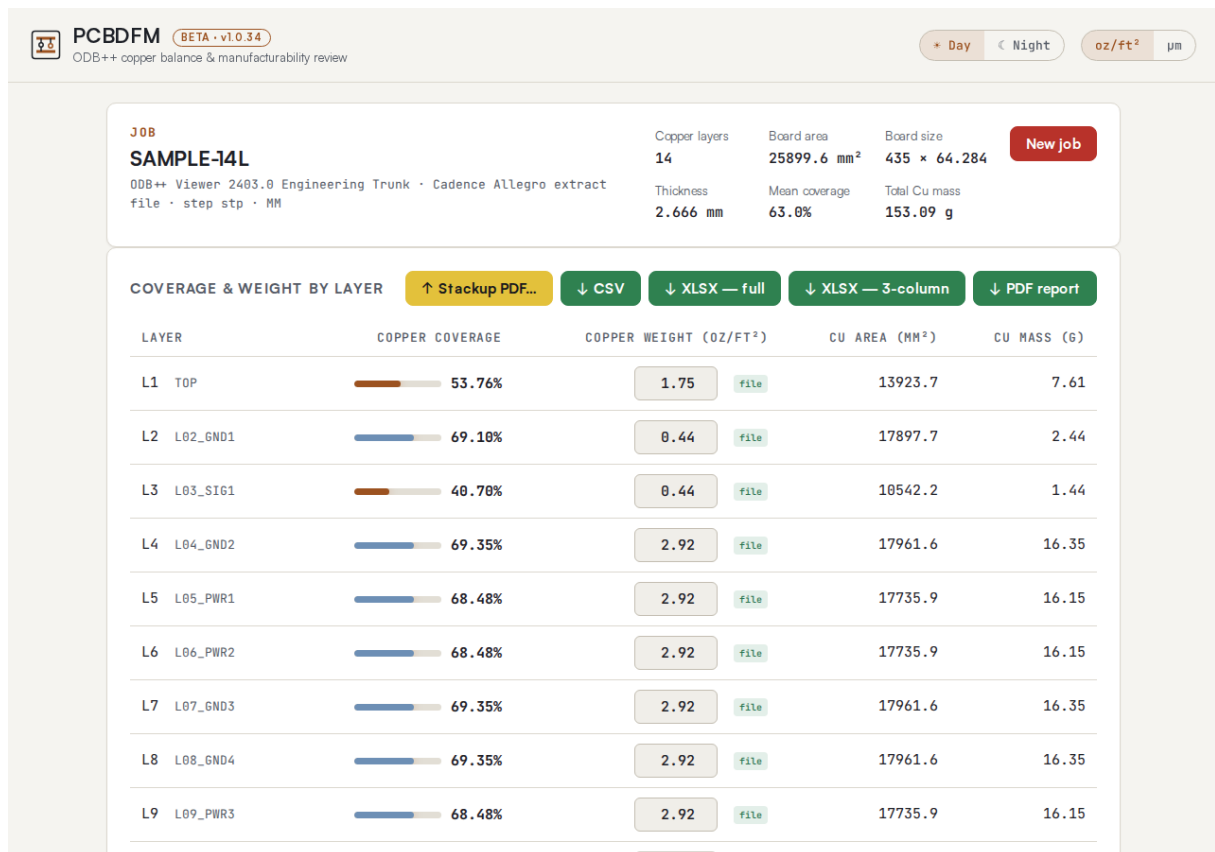


Figure 4 — Job summary and coverage and weight by layer

What is shown

- **Job summary:** job name, source CAD system, number of copper layers, board area and size, thickness, mean coverage and total copper mass.
- **Coverage and weight by layer:** one row per copper layer from L1 to the last layer with copper coverage (%), copper weight, copper area (mm²) and copper mass (g). Coverage is copper area ÷ board profile area.
- **Weight source tag:** file (read from the job), pdf (read from a drawing's stack legend) or manual (typed by you).
- **Units:** the oz/ft² and µm switch at the top right changes how weights are shown and entered (1 oz/ft² = 34.79 µm).
- **Day / Night:** the ☀ Day and 🌙 Night switch at the top right sets a bright or dark background. PCBDFM always opens in Day (bright); the choice lasts while the tab is open and is not stored in the browser.
- **Language:** the flag button at the top right opens the language menu: English (UK flag), Tiếng Việt, 中文（简体）, 日本語, 한국어, Español, Français and Deutsch. The screen, the PDF and Excel reports and this manual follow the language chosen. PCBDFM always opens in English; the choice lasts while the tab is open and is not stored in the browser. Numbers, units, layer and net names, IPC references and RED FLAG are the same in every language, and text quoted from the customer's data (drawing notes, vendor names) is shown as written. The language can be changed at any time, even while a job is being analysed or reviewed; the reports are written in the language selected when they are downloaded.



Figure 5 — Language menu

Outer-layer copper weight. Outer layers are plated up together with the holes, so the weight stated for an outer layer is the finished weight — starting foil plus plating. For example, “1 oz” outer means 1 oz finished. PCBDFM uses the stated outer weight as the finished copper for all etching rules.

Missing copper weights

If the job does not carry a copper weight for some layers, those rows are highlighted and a panel lets you enter outer and inner weights, apply them to blank rows or overwrite all, or pick a preset (½/½ oz, 1/½ oz, 1/1 oz, 2/1 oz). You can also type a weight directly into any row. Totals and balance update immediately.

Stack symmetry

Layers are paired from the outside in (L1 ↔ L-last, L2 ↔ L-last-1 ...). For each pair PCBDFM shows the difference in percentage points and the true relative difference:

$$\Delta \text{ true (\%)} = (\text{heavier} - \text{lighter}) \div \text{lighter}$$

When both weights are known the comparison uses copper quantity (coverage × copper thickness). Under about 20% is comfortable; above about 50% drives lamination and reflow warpage.

L1 / L12		1.59 pts	2.09%
L2 / L11		0.11 pts	0.12%
L3 / L10		0.23 pts	0.26%
L4 / L9		0.00 pts	0.00%
L5 / L8		1.22 pts	2.47%
L6 / L7		0.57 pts	0.63%

Figure 6 — Stack symmetry by mirrored pair

Findings

A short list of copper-balance observations follows: low-coverage layers, unbalanced pairs, outer versus inner loading and missing data.

- Largest mirrored-pair difference is 1.22 pts (L5/L8) — the heavier side carries 2.47% more copper. Well inside the comfortable range for warpage control.
- Outer copper averages 77.0% against 82.2% on the inners — no unusual etch/plating loading split.
- Every layer has a copper weight, so mass and total copper are complete.

Figure 7 — Copper balance findings

5. Stage 2 — DFM full design review

Below the copper balance is the DFM review panel. Choose what to check against (section 5.1), then click Run DFM review. A progress bar shows each stage; large boards take a few minutes.

DFM REVIEW

Vias and drill spans, etching against copper weight, rings and clearances, stackup, solder mask and data completeness — the issues that make a fab no-bid. Uses the copper weights in the table above, and the vendor's limits if you add them below.

☐ Edge plating specified

Reviewing... 36%

36%

Merging copper by net

Capability basis

Choose: Typical defaults · Vendor file · Enter manually

Locked during review

Sierra Proto Express (Sierra Circuits) · 12 limits

Figure 8 — DFM review running

5.1 Check against — the capability menu

The Capability basis menu decides which limits the review uses. Pick one of three options:

Option	What it does	When to use it
Typical defaults	Every check uses typical fab screening values. The values are shown in the table for reference.	Early design checks, or when no fabricator has been chosen yet.
Vendor file	Load the fabricator's completed capability workbook (.xlsx) or its IPC-1710A profile (PDF or Word). The values found are filled into the table with their source, and workbook tables — trace and space per copper weight, drill and aspect ratio per board thickness, laser depth — are applied as well. You can check and correct any value.	Before release to a specific fabricator.
Enter manually	Type the fabricator's limits yourself. Blank fields use the typical value (shown greyed).	When the vendor has given limits by e-mail or on a call.

▼

Capability basis

Hide

Typical defaults

Choose: Typical defaults · Vendor file · Enter manually

Typical defaults

Screening values for a typical fab

Vendor file

Capability workbook (.xlsx) or IPC-1710A (PDF, Word)

Enter manually

Type the vendor's values

Every check uses typical fab screening values (shown below). Choose Vendor file or Enter manually to check against a specific fab.

Vendor library

Choose a published vendor survey..

Use in review

Download survey (.xlsx)

Surveys compiled from each manufacturer's public capability data (sources listed in each workbook). They are not completed or confirmed by the vendor — ask the fab for its signed profile before release.

PARAMETER	VALUE	SOURCE
BOARD		
Maximum copper layers	-	layers Not checked
Minimum board thickness	-	mm Not checked
Maximum board thickness	-	mm Not checked

Figure 9 — Capability basis: Typical defaults

▼

Capability basis

Hide

Vendor file — none loaded

Choose: Typical defaults · Vendor file · Enter manually

Typical defaults

Screening values for a typical fab

Vendor file

Capability workbook (.xlsx) or IPC-1710A (PDF, Word)

Enter manually

Type the vendor's values

Load the fab's completed capability workbook (.xlsx) or its IPC-1710A profile (PDF or Word). Workbook tables — trace and space per copper weight, drill and aspect ratio per board thickness, laser depth — are applied as well as the values below. Check and correct them. Blank fields use typical values. Lengths in mm — type .004" or 4 mil to enter inches. Drill sizes are actual drill sizes.

Choose vendor file...

Clear values

Blank questionnaire (.xlsx)

Vendor

Name

Profile date

Vendor library

Choose a published vendor survey..

Use in review

Download survey (.xlsx)

Surveys compiled from each manufacturer's public capability data (sources listed in each workbook). They are not completed or confirmed by the vendor — ask the fab for its signed profile before release.

PARAMETER	VALUE	SOURCE
BOARD		
Maximum copper layers	-	layers Not checked

Figure 10 — Capability basis: Vendor file

Capability basis
Choose: Typical defaults • Vendor file • Enter manually

Hide

Manual – no values yet

Typical defaults
Screening values for a typical fab

Vendor file
Capability workbook (.xlsx) or IPC-T710A (PDF, Word)

Enter manually
Type the vendor's values

Type the fab's limits. Blank fields use typical values (greyed). Lengths in mm — type .004" or 4 mil to enter inches. Drill sizes are actual drill sizes.

Clear values

↓ Blank questionnaire (.xlsx)

Vendor

Name

Profile date

—

Vendor library

Choose a published vendor survey...

Use in review

↓ Download survey (.xlsx)

Surveys compiled from each manufacturer's public capability data (sources listed in each workbook). They are not completed or confirmed by the vendor — ask the fab for its signed profile before release.

PARAMETER	VALUE	SOURCE
BOARD		
Maximum copper layers	— layers	Not checked
Minimum board thickness	— mm	Not checked
Maximum board thickness	— mm	Not checked
Maximum board size (diagonal)	— mm	Not checked
Maximum copper weight	— oz	Not checked
DRILLING		
Minimum mechanical drill (actual)	0.15 mm	Typical
Minimum laser drill (actual)	0.075 mm	Typical

Figure 11 — Capability basis: Enter manually (first part of the table)

Values that can be set from a vendor file or entered manually:

Group	Parameters
Board	Maximum copper layers; minimum and maximum board thickness; maximum board size (diagonal); maximum copper weight
Drilling	Minimum mechanical drill and minimum laser drill (actual drill sizes); maximum aspect ratio for through holes — standard and advanced — and for blind / microvias; via and component-hole drill allowances (finished + allowance = drill, may be negative)
Via technology	Blind vias, buried vias, laser microvias — yes or no
Etching	Inner and outer minimum clearance and minimum conductor width; inner and outer process allowance per side; whether the allowance scales per oz of copper; outer layer base (starting) foil — a drop-down: ½ oz (default), ¼, ⅜, 1 or 2 oz; whether the outer layers are pattern plated; plane to pad / trace and split-plane gap (default 0.152 mm, 6 mil); outer-layer thermal-relief clearance (0.152 mm); thermal-relief spoke width for component holes on planes (0.20 mm); flex / rigid-flex minimum trace and space (0.089 mm, 3.5 mil)
Holes	Minimum annular ring (from the actual drill); minimum hole wall to copper; non-plated hole wall to copper (default 0.25 mm)
Solder mask	Minimum solder mask dam; solder mask registration tolerance (± 0.05 mm by default) used for the SMD / NSMD pad check
Outline	Outer layer copper to board edge (default 0.25 mm) and inner layer copper / planes to board edge (default 0.381 mm, 15 mil), set separately; copper to a V-score line (0.508 mm, 20 mil); copper to tab / mouse-bite holes (0.254 mm, 10 mil)

Group	Parameters
Legend	Legend (silkscreen) to exposed copper (default 0.203 mm, 8 mil)
RF	RF / microwave boards only: via to other-net copper and stitching via to the edge of its pour (default 0.508 mm, 20 mil each)

Lengths are in mm; type .004" or 4 mil to enter inches. Drill sizes are always actual drill sizes. Clear values empties the table; Blank questionnaire (.xlsx) downloads the empty workbook.

A completed vendor survey sets the board-edge limits (inner and outer separately), the non-plated hole to copper limit, the legend clearance, the V-score clearance and the tab clearance from its Etching, Mechanical Drill, Solder Mask & Legend and Profile & Panel sheets. Values it does not give keep the typical default, shown greyed.

Confirmed design rules

The Confirmed design rules drop-down, above the password-protected library, is open to every user with no password. It holds the vendor rules that have been checked against the manufacturer's published design guides: Sierra Circuits (Sunnyvale, USA) and AdvancedPCB (USA). Choose one, then Use in review to load it as the vendor file, or Download rules (.xlsx) to save the workbook.



Figure 12 — Confirmed design rules, no password needed

Vendor library

The Vendor library is password protected. Enter the library password and choose Unlock; the server checks the password and opens the library for that browser tab for up to two hours. Nothing is stored in the browser, so a new tab or a reload needs the password again. After five wrong passwords the library is locked for 10 minutes. For a password, text an access request to +1 (408) 518 1496.

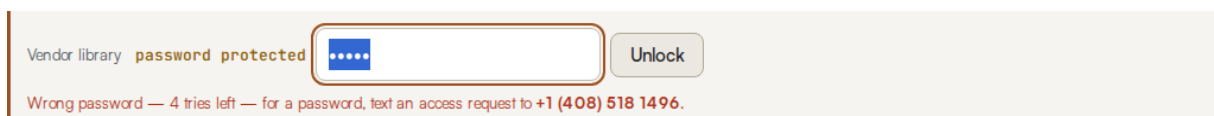


Figure 13 — Vendor library locked (after a wrong password)

The Vendor library under the Vendor file buttons holds capability surveys already filled in for leading PCB manufacturers. Choose a vendor, then Use in review to load its survey as the vendor file, or Download survey (.xlsx) to save the workbook. Each survey is named after the company and location.

- The surveys were compiled from each manufacturer's own public website: capability charts, process-capability tables and technology roadmaps. Every value is in the survey workbook with the page it came from: the Notes column on each sheet and a Sources sheet list the value as published, its unit and the source address.

- Lengths are converted to mm. Where a page gives one value it is entered as Standard production; where it gives mass-production and sample (or normal and advanced) values, both columns are filled.
- Where the website does not say which plant the values apply to, the location is the country and the survey is marked company-level data.
- Manufacturers whose own websites publish no capability values, or fewer than ten, have no survey. The library covers the top 100 PCB manufacturers by 2024 revenue and every other maker in the 2025 list of the 168 fabricators with more than \$100 million in PCB revenue; 64 surveys from 53 companies met the threshold. Version 1.0.54 adds five surveys for TTM's current Asian PCB plants (Dongguan, Guangzhou, Huiyang, Zhongshan and Penang) on request; TTM publishes few numbers per plant, so these surveys hold mainly certificates and listed capabilities, with the gaps left for the vendor. The former TTM Shanghai survey is now listed as AKM Meadville (Shanghai), because TTM sold that plant in 2020. The library holds 69 surveys. Some listed companies, such as NCAB and ICAPE, supply boards through partner factories; their surveys give the capability they publish for those factories.
- A published survey is not the fabricator's confirmed profile. Send the blank questionnaire to the fab and use its completed workbook before release.

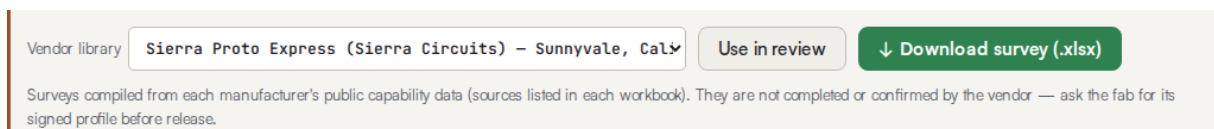


Figure 14 — Vendor library in the Capability basis panel

Company	Location	Values
Aikokiki Manufacturing	Japan (plant not stated)	15
AKM Meadville	China (plant not stated)	8
Aoshikang Technology (ASKPCB)	China (plant not stated)	14
APCT	USA (plant not stated)	24
APCT (AdvancedPCB, formerly Advanced Circuits)	USA (plant not stated)	52
Apex Circuit (Apex PCB)	Thailand	30
AT&S	Nanjangud (Mysuru), India	17
Camelot Electronics	China (plant not stated)	25
Compeq Manufacturing	Taiwan (plant not stated)	15
Daisho Denshi	Japan (plant not stated)	12
Dongshan Precision (DSBJ)	China (plant not stated)	10
Dynamic Electronics	Taiwan (plant not stated)	13
Edadoc	Zhuhai, China	33
Firan Technology Group (FTG)	Toronto (Scarborough), Canada	38
Gorilla Circuits	San Jose, California, USA	23
Gorilla Circuits	USA (plant not stated)	53

Company	Location	Values
Guangdong Champion Asia Electronics	China (plant not stated)	65
Guangdong Kingshine Electronic	China (plant not stated)	11
Gul Technologies (GulTech)	Jiangsu Plant I, China	18
Gul Technologies (GulTech)	Jiangsu Plant II, China	10
Gul Technologies (GulTech)	Singapore (plant not stated)	29
Gul Technologies (GulTech)	Suzhou, China	10
HannStar Board	Taiwan (plant not stated)	64
Huizhou China Eagle Electronic (CEE)	China (plant not stated)	10
ICAPE Group	Europe (plant not stated)	27
ICAPE Group (ICAPE TraX)	Cape Town, South Africa	57
KCE Electronics	Thailand (plant not stated)	56
Kingsignal Technology (Kingsignal Circuit)	China (plant not stated)	46
Kinwong Electronic	China (plant not stated)	23
Liang Dar Technology	Taiwan (plant not stated)	27
Lianjincheng Technology (LJC PCB)	China (plant not stated)	55
Meiko Electronics	Japan (plant not stated)	10
Nan Ya PCB	Taiwan (plant not stated)	28
NCAB Group	Europe (plant not stated)	48
OKI Circuit Technology	Japan (plant not stated)	16
Olympic Circuit Technology	China (plant not stated)	45
PCB Technologies	Israel (plant not stated)	14
Rayben Technology	China (plant not stated)	13
Sanmina	USA (plant not stated)	16
Shengyi Electronics	China (plant not stated)	31
Shennan Circuits	China (plant not stated)	37
Shenzhen Hopesearch PCB	China (plant not stated)	29
Shenzhen Jialichuang Technology (JLCPCB)	China (plant not stated)	74
Shenzhen Jove Enterprise	China (plant not stated)	82
Shenzhen Kingbrother Electronics	China (plant not stated)	42
Shenzhen Lianchuang Electronics (LC PCB)	Shenzhen (Songgang, Bao'an), China	84
Shirai Electronics	Japan (plant not stated)	11
Sierra Proto Express (Sierra Circuits)	Sunnyvale, California, USA	100
Stariver Circuits (Shenzhen Galaxy)	Shenzhen (Shajing, Bao'an), China	28
STARTEAM Global	Germany (plant not stated)	21

Company	Location	Values
Summit Interconnect	USA (plant not stated)	77
Sunshine Global Circuits	China (plant not stated)	59
Suntak Technology	China (plant not stated)	10
Suntak Technology	Jiangmen F2 (Jiangmen Chongda Circuit), China	13
Suntak Technology	Shenzhen, China	12
Suntak Technology	Zhuhai F2, China	12
Tianjin Printronics	China (plant not stated)	12
TLB Co	Korea (plant not stated)	10
Top Reach (Shenzhen Zhichenghe)	China (plant not stated)	18
TTM Technologies	Shanghai, China	17
TTM Technologies	Toronto, Canada	22
TTM Technologies	USA (plant not stated)	45
Würth Elektronik	Germany (plant not stated)	34
Zhejiang Leuchtek	China (plant not stated)	44

5.2 Results

When the review finishes, PCBDFM shows an overall verdict, counts by severity, the issue list with evidence and recommended fixes, the via span table, the dielectric balance tables, the etching-by-layer table and notes about the data. Dielectric balance lists every dielectric between copper layers with its type (prepreg or core), pressed thickness, the resin needed to fill the etched-away copper of the adjacent inner layers and the fill ratio (resin needed ÷ pressed thickness; above 50% risks resin starvation), then compares each mirrored pair for type, thickness and resin draw using the same Δ true bands as copper balance. Cores and unetched outer foil draw no resin. For each copper layer the etching table counts the traces and the gaps below the RED FLAG limit and below the rule, with the narrowest trace and the minimum gap; the Excel export lists every trace width by layer on its Trace widths sheet. Under the table the report draws a map for every copper layer, inner or outer, that has an exception: gaps below the rule are marked by band (Query and RED FLAG) and traces narrower than the rule as triangles, with the parts nearest the exceptions listed. The Excel register gives every location: a Spacing sheet for each layer with gaps and a Narrow traces sheet with each narrow trace (layer, width, position, nearest part and status). The Rule basis column shows where each layer's limits came from: Vendor (the vendor's trace and space for that copper weight) or Typical † (the vendor gives none for that weight, so typical-fab values are used; ask the vendor before relying on those calls). The Excel register has the same table on its Etching sheet, and its Spacing and Trace widths sheets give the rule basis for every listed gap and width.

↓ DFM report PDF
↓ Issue register XLSX

Capability basis
Choose: Typical defaults · Vendor file · Enter manually

Change

Sierra Proto Express (Sierra Circuits) · 12 Limits

Not manufacturable as released
At least one issue is enough on its own for a fab to decline to quote.

2 No-bid
1 HoLd
17 Query
8 Cost

#	ISSUE	SEVERITY	EVIDENCE	FIX
1	Via spans too deep to drill and plate	No-bid	1,56.5 vias in 1 span(s) (L1—L14), aspect ratio 10.5—10.5:1	Convert to through vias, or re-plan as stacked/staggered microvias of ≤ 1:1 per step
2	top: features too fine for 61 µm finished (incl. plating) copper	No-bid	68.4 traces < 0.125 mm — typical-fab rule: the vendor gives no trace and space for this copper weight	Reduce copper on top, or open gaps to ≥ 0.18 mm and traces to ≥ 0.15 mm
3	Copper artwork outside the board outline	HoLd	16,946 features, 310 mm² on top (I230), I02_gnd1 (I198), I03_sig1 (I209), I04_gnd2 (I198), I05_pwr1 (I188), I06_pwr2 (I209), I07_gnd3 (I207), I08_gnd4 (I213), I09_pwr3 (I211), I10_pwr4 (I176), I11_gnd5 (I183), I12_sig2 (I196), I13_gnd6 (I288), bottom (I264)	Move drawings/tables to a documentation layer before export
4	top: copper heavier than the vendor's etch table	Query	61 µm; no row in the vendor's trace/space table covers it — typical rules used (Sierra Proto Express (Sierra Circuits) capability workbook)	Ask the vendor for trace and space at this copper weight
5	top: below typical-fab rules (no vendor value for this copper) for 61 µm finished (incl. plating)	Query	64 gaps 0.125—0.180 mm	Fab may accept with etch compensation at extra cost; confirm with the fab
6	I04_gnd2: copper heavier than the vendor's etch table	Query	102 µm; no row in the vendor's trace/space table covers it — typical rules used (Sierra Proto Express (Sierra Circuits) capability workbook)	Ask the vendor for trace and space at this copper weight
7	I05_pwr1: copper heavier than the vendor's etch table	Query	102 µm; no row in the vendor's trace/space table covers it — typical rules used (Sierra Proto Express (Sierra Circuits) capability workbook)	Ask the vendor for trace and space at this copper weight
8	I06_pwr2: copper heavier than the vendor's etch table	Query	102 µm; no row in the vendor's trace/space table covers it — typical rules used (Sierra Proto Express (Sierra Circuits) capability workbook)	Ask the vendor for trace and space at this copper weight
9	I07_gnd3: copper heavier than the vendor's etch table	Query	102 µm; no row in the vendor's trace/space table covers it — typical rules used (Sierra Proto Express (Sierra Circuits) capability workbook)	Ask the vendor for trace and space at this copper weight
10	I08_gnd4: copper heavier than the vendor's etch table	Query	102 µm; no row in the vendor's trace/space table covers it — typical rules used (Sierra Proto Express (Sierra Circuits) capability workbook)	Ask the vendor for trace and space at this copper weight
11	I09_pwr3: copper heavier than the vendor's etch table	Query	102 µm; no row in the vendor's trace/space table covers it — typical rules used (Sierra Proto Express (Sierra Circuits) capability workbook)	Ask the vendor for trace and space at this copper weight
12	I10_pwr4: copper heavier than the vendor's etch table	Query	102 µm; no row in the vendor's trace/space table covers it — typical rules used (Sierra Proto Express (Sierra Circuits) capability workbook)	Ask the vendor for trace and space at this copper weight
13	I11_gnd5: copper heavier than the vendor's etch table	Query	102 µm; no row in the vendor's trace/space table covers it — typical rules used (Sierra Proto Express (Sierra Circuits) capability workbook)	Ask the vendor for trace and space at this copper weight
14	bottom: copper heavier than the vendor's etch table	Query	61 µm; no row in the vendor's trace/space table covers it — typical rules used (Sierra Proto Express (Sierra Circuits) capability workbook)	Ask the vendor for trace and space at this copper weight
15	bottom: below typical-fab rules (no vendor value for this copper) for 61 µm finished (incl. plating)	Query	1 gap 0.125—0.180 mm	Fab may accept with etch compensation at extra cost; confirm with the fab
16	Copper land on non-plated holes	Query	22 non-plated holes have copper reaching the hole (e.g. drill 3.00 mm at -2.00, -10.00 on bottom)	Confirm an unsupported land is intended; otherwise pull copper back ≥ 0.25 mm or make the hole plated
17	top: uneven copper density	Query	17 mm cells 7—100%, standard deviation 25 pts, 18 cells under 25%	Add thickening in open areas for even plating on outer layers
18	bottom: uneven copper density	Query	17 mm cells 6—100%, standard deviation 25 pts, 14 cells under 25%	Add thickening in open areas for even plating on outer layers
19	Top mask webs too thin	Query	33 webs < 0.100 mm (Sierra Proto Express (Sierra Circuits) capability workbook)	Gang the openings or reduce mask expansion
20	Bot mask webs too thin	Query	9 webs < 0.100 mm (Sierra Proto Express (Sierra Circuits) capability workbook)	Gang the openings or reduce mask expansion

Figure 15 — DFM verdict and issue list

VIA SPANS

SPAN	TYPE	HOLES	DRILL	ASPECT	VERDICT
L1-L14	through	1,585	0.250	10.5:1	Not buildable

DIELECTRIC BALANCE

Prepreg is the only dielectric that flows at lamination; it fills the copper etched away on the adjacent inner layers. Resin needed = $\Sigma (1 - \text{coverage}) \times \text{copper thickness of those layers}$; fill = resin needed $\div$ pressed thickness, above 50% risks starvation. Cores and unetched outer foil draw no resin. Mirrored dielectrics should match in type, thickness and resin draw.

DIELECTRIC	BETWEEN	TYPE	PRESSED (μm)	RESIN NEEDED (μm)	FILL	RATING
D1	L1-L2	prepreg *	98	5	5%	OK
D2	L2-L3	core *	127	—	—	Core (no flow)
D3	L3-L4	prepreg *	158	40	26%	OK
D4	L4-L5	core *	102	—	—	Core (no flow)
D5	L5-L6	prepreg *	155	64	41%	OK
D6	L6-L7	core *	102	—	—	Core (no flow)
D7	L7-L8	prepreg *	155	62	40%	OK
D8	L8-L9	core *	102	—	—	Core (no flow)
D9	L9-L10	prepreg *	155	64	41%	OK
D10	L10-L11	core *	102	—	—	Core (no flow)
D11	L11-L12	prepreg *	158	40	25%	OK
D12	L12-L13	core *	127	—	—	Core (no flow)
D13	L13-L14	prepreg *	98	5	5%	OK

MIRRORED DIELECTRIC PAIRS

PAIR	TYPE	PRESSED (μm) UPPER / LOWER	RESIN (μm) UPPER / LOWER	Δ TRUE RESIN	RATING
D1 ↔ D13	prepreg	98 / 98	5 / 5	0.8%	OK
D2 ↔ D12	core	127 / 127	—	—	OK
D3 ↔ D11	prepreg	158 / 158	40 / 40	1.1%	OK
D4 ↔ D10	core	102 / 102	—	—	OK
D5 ↔ D9	prepreg	155 / 155	64 / 64	0.0%	OK
D6 ↔ D8	core	102 / 102	—	—	OK

Δ true resin = (heavier – lighter) $\div$ lighter on resin needed, same bands as copper balance. Thickness more than 5 μm apart, or a prepreg mirrored by a core, is asymmetric. D7 is the centre dielectric and has no mirror. * Type assumed from the standard foil build — confirm with the fab stack-up.

Figure 16 — Via spans and dielectric balance

ETCHING BY LAYER											
LAYER	COPPER	TRACE / GAP	RULE	NO-BID	TRACES	TRACES	NARROWEST	GAPS	GAPS	MIN	RULE
				TRACE / GAP	< NO-BID	< RULE	TRACE	< NO-BID	< RULE	GAP	BASIS
top	61 µm fin.	0.150 / 0.180	0.125 / 0.125	0.125 / 0.125	684	684	0.102	0	64	0.149	Typical †
l02_gnd1	15 µm	0.050 / 0.083	0.050 / 0.075	0.050 / 0.075	0	0	0.650	0	0	—	Vendor ½ oz
l03_sig1	15 µm	0.050 / 0.083	0.050 / 0.075	0.050 / 0.075	0	0	0.102	0	0	0.148	Vendor ½ oz
l04_gnd2	102 µm	0.200 / 0.250	0.175 / 0.175	0.175 / 0.175	0	0	0.650	0	0	—	Typical †
l05_pwr1	102 µm	0.200 / 0.250	0.175 / 0.175	0.175 / 0.175	0	0	0.650	0	0	—	Typical †
l06_pwr2	102 µm	0.200 / 0.250	0.175 / 0.175	0.175 / 0.175	0	0	0.650	0	0	—	Typical †
l07_gnd3	102 µm	0.200 / 0.250	0.175 / 0.175	0.175 / 0.175	0	0	0.650	0	0	—	Typical †
l08_gnd4	102 µm	0.200 / 0.250	0.175 / 0.175	0.175 / 0.175	0	0	0.650	0	0	—	Typical †
l09_pwr3	102 µm	0.200 / 0.250	0.175 / 0.175	0.175 / 0.175	0	0	0.650	0	0	—	Typical †
l10_pwr4	102 µm	0.200 / 0.250	0.175 / 0.175	0.175 / 0.175	0	0	0.650	0	0	—	Typical †
l11_gnd5	102 µm	0.200 / 0.250	0.175 / 0.175	0.175 / 0.175	0	0	0.650	0	0	—	Typical †
l12_sig2	15 µm	0.050 / 0.083	0.050 / 0.075	0.050 / 0.075	0	0	0.102	0	0	0.142	Vendor ½ oz
l13_gnd6	15 µm	0.050 / 0.083	0.050 / 0.075	0.050 / 0.075	0	0	0.650	0	0	—	Vendor ½ oz
bottom	61 µm fin.	0.150 / 0.180	0.125 / 0.125	0.125 / 0.125	0	0	0.150	0	1	0.171	Typical †

Rule basis: Vendor = the vendor's trace and space for that copper weight; Typical † = the vendor gives none for that weight, so typical-fab values are used — ask the vendor before relying on those calls.

- Dielectric type (core / prepreg) is not in the data — the standard foil build is assumed (prepreg next to the outer layers, then core and prepreg alternating). Resin fill is checked on prepreg gaps only; confirm against the fab stack-up.
- Drill basis: the drill table lists FINISHED hole sizes (drill table on layer fab, FINISHED sizes). An oversized drill was used for this assessment of the 1,585 plated holes to allow for plating: the designer's stated tool size for 405 (0.2286 → 0.3048 mm = finished + 0.0762 mm); finished + 0.05 mm plating allowance for 1,180. The 22 non-plated holes were assessed at their listed size, which is the actual drill.

Figure 17 — Etching by layer and notes

Verdict	Meaning
Not manufacturable as released	At least one RED FLAG issue — enough on its own for a fab to decline to quote.
Buildable after corrections	No hard stop, but CAM would put the job on hold until the Hold items are answered.
Buildable with engineering queries	Expect questions from the fab before quoting; none is a blocker on its own.
No blocking issues found	All checks pass at the selected capability.

Severity	Meaning
RED FLAG	The fabricator cannot build it as drawn.
Hold	Must be corrected or answered before the job is released to production.
Query	The fabricator will ask about it; may be accepted with confirmation.
Cost	Buildable, but adds process steps or cost.

Copper density maps. The DFM report PDF shows the copper coverage of every layer as a map of cells across the board, one row per mirrored pair (L1/Ln, then L2/Ln-1 and so on), on the same colour scale. Under each pair it gives the range and spread of coverage for both layers and how much the two differ cell by cell, with the location of the largest difference. A light area on one layer

opposite a heavy area on its mirror is where the panel is most likely to bow or twist. The issue register has the same figures in the Density pairs and Density cells sheets.

Copper density by mirrored pair

Each map shows the copper coverage of one layer in cells across the board, seen from the top. Mirrored layers are shown side by side on the same scale, so a light area on one and a heavy area on the other at the same spot shows local imbalance through the thickness.

L1 / L12 — outer pair

- L1 top: 25 mm cells range 35–94% (standard deviation 16 pts, 0 of 51 cells under 25%).
- L12 bottom: 25 mm cells range 33–94% (standard deviation 18 pts, 0 of 51 cells under 25%).
- Cell by cell the pair differs by 11 pts on average; the largest difference is 38 pts near X 188, Y -7 mm (L1 heavier); 9 of 51 cells differ by more than 30 pts.
- Uneven outer density over-plates sparse areas and under-plates dense ones; add thieving in open areas where clearances allow.

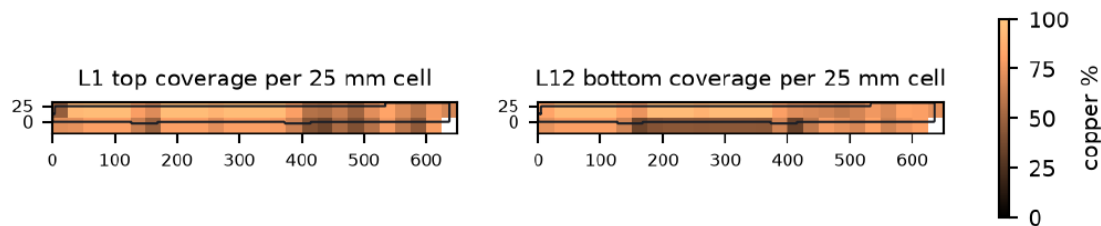


Figure 18 — Copper density maps for a mirrored pair (DFM report PDF)

6. Checks that are made

The DFM review runs every check on the actual geometry of every copper layer. Distances are measured to 0.001 mm.

Drill basis — the actual drill

All hole checks use the actual drill that makes the hole, never a smaller finished size:

- The drill table is looked for in three places, in this order: the ODB++ drill tool table, a drill chart drawn on a layer inside the job, then the drill table on an uploaded fabrication drawing PDF. A drawing note such as “Finished hole size shall be per the drill table” counts as stating finished sizes.
- If no drill table states finished sizes, the listed size is the drill size.
- If the drill table states finished sizes for plated holes, the finished size includes the hole-wall plating, so a larger drill is used: the designer’s tool size where the table gives one (the report shows, for example, “drill chart tool size = finished + 0.0762 mm plating allowance”), otherwise the finished size + 0.05 mm (+ 0.002 in on inch drawings) plating allowance.
- Non-plated holes are always assessed at their listed size, which is the actual drill.
- Backdrills are recognised: the via plating is removed on the backdrilled layers, so those layers are not counted for the via’s ring and clearance.

The reports state which basis was used and list every hole size with the drill used for the checks. Because a finished-size hole uses a bigger drill, this directly affects annular rings and inner-layer clearances.

Fab drill list

The Fab drill list panel takes the fabricator's own finished-to-drill list, either pasted (one pair per line, e.g. "0.2032 0.1803" or "8 mil 7.1 mil") or dropped in as a CSV, text, Excel or PDF file (the file is read and deleted at once). For plated holes with finished sizes the drill is taken, in this order, from: the fab drill list, the vendor's via or component-hole drill allowance, then the drill rule above. The report says how many holes used each source. A list that matches no hole size is reported in the notes.

Outer copper: base foil and pattern plating

Outer layers are always plated up, so a stated outer copper weight is the finished weight. The fine-line limit on a pattern-plated outer layer is set by the base (starting) foil that is etched, not by the finished thickness:

- The base foil defaults to ½ oz (17.5 µm), the usual multilayer outer foil. Choose another weight from the Outer layer base (starting) foil drop-down in the capability table (¼, ¾, 1 or 2 oz); it works in every capability mode.
- If no foil is chosen and the finished outer copper is too thin for ½ oz plus plating, the lighter foil is used; if it is 2 oz finished or heavier, the heavier foil is used. A data note says so.
- Plating is the hole-wall plating (25 µm unless the vendor gives it) plus any cap plating stated on the drawing (e.g. "COPPER CAP PLATING TO BE MINIMUM 13UM").
- Lines finer than the finished-copper rule but within the base-foil limit are a Query — "fine lines need etch compensation (slight modification)"; below the base-foil limit they are a RED FLAG. With a vendor table, the vendor's row for the base foil is used.

Board outline, rails and thickness

- Break-away rails joined by tabs are recognised: the board inside the rails is reviewed and used for copper area, coverage and density. The rails are shown on screen and in the reports.
- Arcs are drawn finely enough that curved track gaps measure as the fab measures them.
- Vector lettering in copper is left out of the conductor widths.
- When the data states a board thickness that differs from the layer stack, the stated thickness is used for through-hole depth and aspect ratio, and the difference is noted.
- Through-hole aspect ratio: up to the vendor's standard ratio is OK; between standard and advanced it is a Query ("at the edge of capability"); beyond advanced it is a RED FLAG.

Same-net spacing, holes in SMD pads and tented vias

- Same-net spacing is reported as information only: for each layer, the closest gap between separate copper shapes of the same net (under 0.2 mm) and how many are below the space rule. It is not a short or an etch defect. Gaps inside one copper shape (a notch between a track and its own pad) are not included.
- Holes in SMD pads: holes inside surface-mount copper pads — pads tagged SMD in the data, and pads under surface-mount package pins (thermal pads), excluding press-fit pins that stand on a component hole. Vias are a Query: confirm fill and cap plating (IPC-4761 Type VII) when the drawing calls for it, otherwise fill and cap or move them. Component holes in SMD pads are a Query. The count of these vias covered by solder mask is given.

- Tented vias: the number of vias covered by solder mask (no mask opening over the hole) on each side and on both sides, as a data note.

Board type

The Board type drop-down in the DFM review panel decides which board-specific rules apply. Auto (the default) decides from the data:

- Flex or rigid-flex: the job has flex layer types (coverlay, covercoat, stiffener, bend area) or layers named for them, or the fabrication drawing mentions coverlay, polyimide, stiffener or rigid-flex. Rigid-flex when there are more than two copper layers.
- RF / microwave: the job or the drawing names an RF laminate (Rogers RO4000 / RO3000, Duroid, PTFE, Taconic, Arlon and similar) or calls the board or a section RF or microwave.
- Rigid otherwise. Choose Rigid, HDI, RF / microwave, Flex or Rigid-flex to override. The data notes in the report state the board type and why.

DFM REVIEW

Vias and drill spans, etching against copper weight, rings and clearances, stackup, solder mask and data completeness — the issues that make a fab decline to quote. Uses the copper weights in the table above, and the vendor's limits if you add them below.

☐ Edge plating specified Board type RF / microwave

Run DFM review

Figure 19 — Board type in the DFM review panel

Flex and rigid-flex boards: no trace or gap below 0.089 mm (3.5 mil) on any layer, whatever the copper weight. RF / microwave boards: vias are checked 0.508 mm (20 mil) from other-net copper, measured from the via wall, and stitching vias 0.508 mm inside the edge of their pour.

Heavy copper

Above 75 μm (about 2 oz) the default etch rules rise with copper weight, and outer layers, etched in foil plus plating, need wider lines than inner layers. RED FLAG limits (trace / gap, mm):

Copper	Inner layers	Outer layers (finished)
to 110 μm (3 oz)	0.178 / 0.203	0.178 / 0.178
to 150 μm (4 oz)	0.203 / 0.254	0.279 / 0.279
to 185 μm (5 oz)	0.229 / 0.279	0.356 / 0.356
to 220 μm (6 oz)	0.254 / 0.305	0.406 / 0.406
heavier	0.254 / 0.305	0.508 / 0.508

Below standard production (about 10 % above these) is a Query. The base-foil relaxation for pattern-plated outer layers is not applied to 2 oz foil and heavier. A vendor's own table always takes precedence.

Edge plating

Copper that reaches the board outline is normally a Hold, because a routed edge cuts through it. When the board is to have edge plating, that copper is intended. The review treats edge plating as specified when any of these is true:

- The uploaded fabrication drawing asks for it: a note such as “Edge plating”, “Plated edge”, “Castellated holes” or “Side plating”. Notes that rule it out, such as “No edge plating” or “Edge plating not required”, do not count. The status line under the drop zone shows the note that was found.
- Edge plating specified is ticked in the DFM review panel. It is ticked automatically when the drawing asks for edge plating, and you can tick or clear it before running the review.
- A layer in the ODB++ job is named for edge plating (for example an edge-plating route layer).

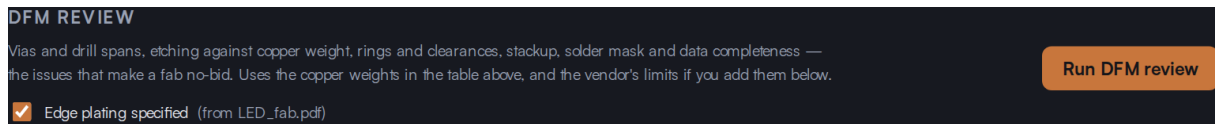


Figure 20 — Edge plating specified, ticked automatically from the fabrication drawing

The report then lists the layers whose copper reaches the outline under one Cost item, Edge plating specified, and the data notes say where it was stated. Check with the fab that copper reaches the outline only on the edges that are to be plated.

Full list of checks

Area	Check	What is reported
Vias and drilling	Via spans and aspect ratio	Every drill span (through, blind, buried) with smallest actual drill, depth and aspect ratio: OK to 8:1, Tight from 8:1 to 10:1, RED FLAG beyond 10:1 for through holes at typical capability; with a vendor, OK to its standard ratio, Query to its advanced ratio, RED FLAG beyond; blind/laser to 1:1 (marginal to 1.4:1). Tented vias are counted
	Minimum drill	Actual drills below the mechanical (0.15 mm) or laser (0.075 mm) limit
	Span sequencing	Blind/buried spans that overlap and cannot be laminated in sequence; different-net vias stacked in plan view
Rings and breakout	Annular ring	Smallest ring from the actual drill on every connected in-span layer, for round holes and slots; holes that break out of the pad and by how much
	Hole wall to copper	Distance from the drilled wall of each plated hole to other-net copper on every in-span layer, inner layers included (planes and anti-pads)
	Non-plated holes	Distance from the drilled wall to any copper (vendor limit, default 0.25 mm), and copper lands on non-plated holes
	Mouse-bite tabs	Three or more small non-plated holes (up to 1 mm) in a row at the outline are tab-routing holes: copper closer than 0.254 mm (10 mil) is a Query
	RF / microwave vias	RF boards only: vias closer than 0.508 mm to other-net copper; stitching vias closer than 0.508 mm to the edge of their pour (Query)
	Backdrill	Backdrill to other-net copper on the backdrilled layers (backdrill assumed actual drill + 0.20 mm when its diameter is not in the data)

Area	Check	What is reported
	Hole to hole	Wall-to-wall spacing between holes with overlapping spans
Copper spacing and etching	Copper-to-copper spacing per layer	Smallest gap between different nets on every layer, measured on the merged copper of each net; copper with no net counts each shape separately
	Conductor width	Narrowest traces on every layer
	Etching against copper weight	Gaps and traces compared with the rule for that layer's copper weight (outer layers at their finished weight); RED FLAG below the minimum, Query below standard production
	Planes	Gaps under 0.152 mm (6 mil) between a plane or pour (any copper shape of 25 mm ² or more) and other-net pads or traces, and between split planes (Query, one item for the board)
	Thermal reliefs	Outer layers: thermal-relief air gaps between a pad and its pour narrower than 0.152 mm (Query)
	Plane connections at component holes	Every through-hole component pin (vias excluded) on every layer where a plane or pour of its own net surrounds the hole: thermal relief (spokes counted, narrowest spoke and air gap measured), solid (direct) connection, or cleared (not connected). Every other through-hole pin without thermal relief is listed in full in the report (Through-hole pins without thermal relief: reference, pin, net, connection, number of planes, layers and position, with a count per part). Solid on two or more planes: Hold; solid on one plane: Query; cleared from its own plane: Hold; spokes under 0.20 mm (or the vendor's value), a single spoke, or an air gap under 0.152 mm: Query. 2–3 spoke reliefs are listed for information. Press-fit pins are recognised from the data (ODB++ mount type press-fit, a package type such as CONN-PF or PRESSFIT, 'press-fit' in the part or package name, or a press-fit drill tool). They are not soldered, so a solid plane connection is expected: they are counted separately and left out of the thermal-relief and mask-to-pad checks. The report names each press-fit connector in a Press-fit connectors table (reference, part, package, side, pins, pins on planes, finished holes with tolerance, and how it was recognised) and raises one Query naming them, to confirm the finished hole size, tolerance (normally ±0.05 mm, read from the drill table) and plating with the connector maker's press-fit specification (IPC-9797). High-current soldered pins are often solid on purpose: confirm with the designer (IPC-2221B 9.1.3)
	V-score	Copper within 0.508 mm (20 mil) of a V-score line on any layer (Hold); score lines are read from a layer named V-SCORE, V-CUT or V-GROOVE. A drawing that calls for V-scoring with no score layer in the data is a Query
	Board edge	Copper closer than the edge limit to the board outline or an internal cut-out — outer layers 0.25 mm, inner layers and planes 0.381 mm by default, or the vendor's values; copper outside the outline. When edge plating is specified, copper that reaches the outline is the plated edge: it is reported once as a Cost item (confirm the plated edges with the fab) instead of a Hold on each layer

Area	Check	What is reported
Stack-up	Symmetry	Mirrored dielectric thicknesses and copper weights
	Prepreg resin fill	For each prepreg gap: resin needed to fill the etched-away copper of the adjacent inner layers versus the pressed thickness; starvation risk when the need exceeds half the thickness. Cores are already cured and are not counted. If the data does not state core or prepreg, the standard foil build is assumed and this is stated in the report
	Copper density	Copper coverage of every layer on a grid, shown as maps for each mirrored pair (L1/Ln, L2/Ln-1 ...) on one scale. Outer pair: uneven areas that plate unevenly (Query). Inner pairs: spots where one layer is much lighter than its mirror, which can bow or twist the panel after lamination (reported with the maps)
	Same-net spacing	Information: closest gap between separate shapes of one net per layer, and how many are below the space rule
	Holes in SMD pads	Vias and component holes inside surface-mount copper pads, with the number covered by mask
Legend	Legend to exposed copper	Legend (silkscreen) ink on or within 0.203 mm (8 mil) of a solder mask opening over copper, per side (Query); openings round non-plated holes only are not counted
Solder mask	SMD and NSMD pads	Every component pad against its mask opening. NSMD (non-mask-defined: the opening clears the pad): the clearance must be at least the mask registration tolerance (0.05 mm, or the vendor's value) so misregistration cannot put mask on the pad. SMD (mask-defined: the opening sits inside the pad): the opening must be at least that far inside the copper all round so it stays fully on the pad. Pads with an opening partly on and partly off the pad, and component pads with no opening, are listed too (all Query). A design exported with 1:1 openings (zero clearance) is flagged: confirm the fab applies its own mask expansion
	Mask webs and via in pad	Mask dams below the minimum; small vias inside component pad openings (fill and cap per IPC-4761 Type VII). Vias in mask openings with no component pad (open copper for heat spreading or shielding) are listed separately and need no fill, as nothing is soldered there
Data	Completeness	Missing outline, copper weights, dielectric thicknesses, nets or fabrication attributes, and any feature that could not be drawn

7. Downloading reports

Every download is generated from your session and saved by your browser to its usual download folder.

Reports are written in the language chosen on the main screen (see Language in section 4, What is shown); a non-English file has the language code at the end of its name, e.g. _DFM_report_vi.pdf. Choosing another language after a review rebuilds the reports in that language without re-running the review, while the results are still on screen. The User manual (PDF) link also opens the manual in the chosen language.

Button colours: yellow buttons with an up arrow upload a file to the review (Select files, Stackup PDF..., Choose vendor file...); green buttons with a down arrow download a file (all report downloads, the blank questionnaire, vendor surveys and the Windows installer). The red New job button clears the current job and its files so you can start again.

Copper balance downloads

These buttons are at the top of the coverage and weight table and are available as soon as the copper balance appears.

Every downloaded report — PDF, Excel and CSV, from the copper balance and from the DFM review — carries the notice “App copyright of John Burke Vietman LLC - manufacturing consultants - for advice call or text John at +1 (408) 518 1496”. In a PDF it is on the footer of every page; in Excel it is two rows below the data on every sheet and in the printed page footer; in a CSV it is the last line.

Button	Format	Contents
CSV	.csv	Layer table: layer, coverage, weight, area and mass
XLSX — full	.xlsx (Excel)	Full workbook: layer table, board facts, stack symmetry pairs and findings
XLSX — 3-column	.xlsx (Excel)	Layer / copper coverage % / copper weight, plus board facts and symmetry pairs
PDF report	.pdf	Copper balance report: layer table, stack symmetry and findings
Stackup PDF...	upload	Not a download — reads copper weights and the drill table from a fabrication drawing PDF

DFM review downloads

These buttons appear next to Run DFM review when the review has finished.

Button	Format	Contents
DFM report PDF	.pdf	Full DFM report: verdict and issue summary, vendor capability basis, copper balance with density maps for every mirrored layer pair, dielectric (prepreg) balance, stack-up drawing with via spans, vias and drilling with the drill basis table, rings and clearances, etching by layer with an exception map for every copper layer that has exceptions (gaps below the rule by band, and narrow traces as triangles, with the worst parts listed under each map), then three dedicated sections — 6 Thermal relief (outer-layer relief gaps and the plane connection of every component hole), 7 Solder mask (SMD / NSMD pads against the registration tolerance, pads partly mask-defined or under mask, mask webs, vias in pads) and 8 Legend ink (legend on or near exposed copper) — and 9 Recommended actions

Button	Format	Contents
Issue register XLSX	.xlsx (Excel)	Workbook with sheets: Summary (all issues with severity, evidence and fix), Vendor capability, Copper balance, Stackup, Dielectric balance, Via spans, Drill basis, Rings & clearance (every location with coordinates, drill and layer, including mouse-bite and RF via rows), Plane connections (every component pin on every plane layer: connection, spokes, narrowest spoke, relief gap, position and whether the pin is press-fit), Mask to pad (every pad outside the SMD / NSMD limits, partly mask-defined or under mask), Other clearances (plane, thermal-relief, V-score and legend locations), Spacing per layer, Edge clearance, Solder mask (vias in component pads and in open copper), Density pairs (coverage statistics and pair differences per layer) and Density cells (the coverage of every grid cell on both layers of each pair, with the difference)

Download before you leave. Design files are deleted when the DFM review finishes. Download the reports you need before starting a new job or closing the tab; to produce them again later you will need to upload the job again.

Only IPC specifications are referenced in the reports. The footer of each PDF and the title row of each workbook carry the PCBDFM version used.

8. Tips and limitations

- Export the ODB++ job with the drill table on the fabrication layer, so the finished-or-drill basis can be read automatically.
- Enter or check copper weights before running the review: etching, ring and resin-fill checks depend on them.
- Add the fabrication drawing PDF before running the DFM review, so its drill table is used. The drawing must contain real text; a scanned image of a drawing cannot be read, and the sizes in the ODB++ drill layers are then used as the actual drill. The message below the job summary confirms when a drill table was found.
- Typical values are screening values for a typical fabricator, not IPC-specified limits. For binding limits load the fabricator's capability file.
- Very large boards (20+ layers, many thousands of holes) can take several minutes; keep the tab open while the review runs.

9. Support

For questions, a desktop download password or help with a review, contact:

John Burke Vietman LLC — manufacturing consultants

Telephone: +1 (408) 518 1496

Web app: <https://pcbdfm.pplx.app>